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A STUDY ON THE DETERMINATION OF MANUFACTURING PROBLEMS SIGNIFICANTLY AFFECTING RELIABILITY OF SILICON PLANAR DEVICES

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FINAL SUMMARY REPORT

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1) INTRODUCTION

The object of this report is to point out, either through actual data or through reports of others in the field, the problems associated with the reliability and yield of planar devices. The devices of primary interest are low, medium and high power transistors and integrated circuits.

When considering reliability and yield, let us begin with an analysis of these two terms. Reliability, can basically be defined as the probability that a piece of equipment, component or system, will successfully perform a specified set of conditions. Usually the definition involves a particular group of limits set by the specific piece of equipment in which the component or sub-system is to operate.

The reliability of an integrated circuit or transistor is a difficult thing to evaluate quantitatively for the reason (assuming high reliability) that the very large numbers needed for testing are not available, and, if they were, would probably be too expensive.

The projected line diagram of Figure 1 is a slightly simplified version of the breakdown of the factors contributing to reliability. The dotted line blocks have been added to show some of the other areas which contribute to reliability but are however not a basic defect in the system or component. The diagram serves to point out that reliability is directly affected by contributions from inherent defects of the materials as well as human error such as that contributed by an operator, jigging or testing and screening procedures.

It is clear from figure 1 that a variety of factors contribute to or subtract from total reliability success and all must be controlled to predict and maximize it. Although we are primarily interested in this report in focusing attention on inherent defects and testing and screening procedures, the human error contributes a significant factor in the overall reliability of the product, however, it is not in this area that the greatest long term increase in reliability is likely to be achieved.

When defining the yield of a particular device or process one may consider it to be that portion or output of the process which will conform to some predetermined set of specifications. Similar to reliability, the yield of a particular device is very closely tied to the number of processing steps to which the component is subjected during the fabrication. In some cases the yield and reliability of a device may be entirely unrelated but quite often they are subject to many of the same processes or reasons for failure. Generally, it has been found that a high yield device is a very reliable device, however, conversely a low yield device is not necessarily an unreliable device. As has been stated before, yield is primarily governed by a set of limits or specifications and these in turn also affect reliability. A device in this respect then will yield a higher percentage of devices for a narrow distribution, but it is difficult to state that a device will be more reliable if it has a broad distribution of parameters.

A number of other definitions which should be included at this point are:

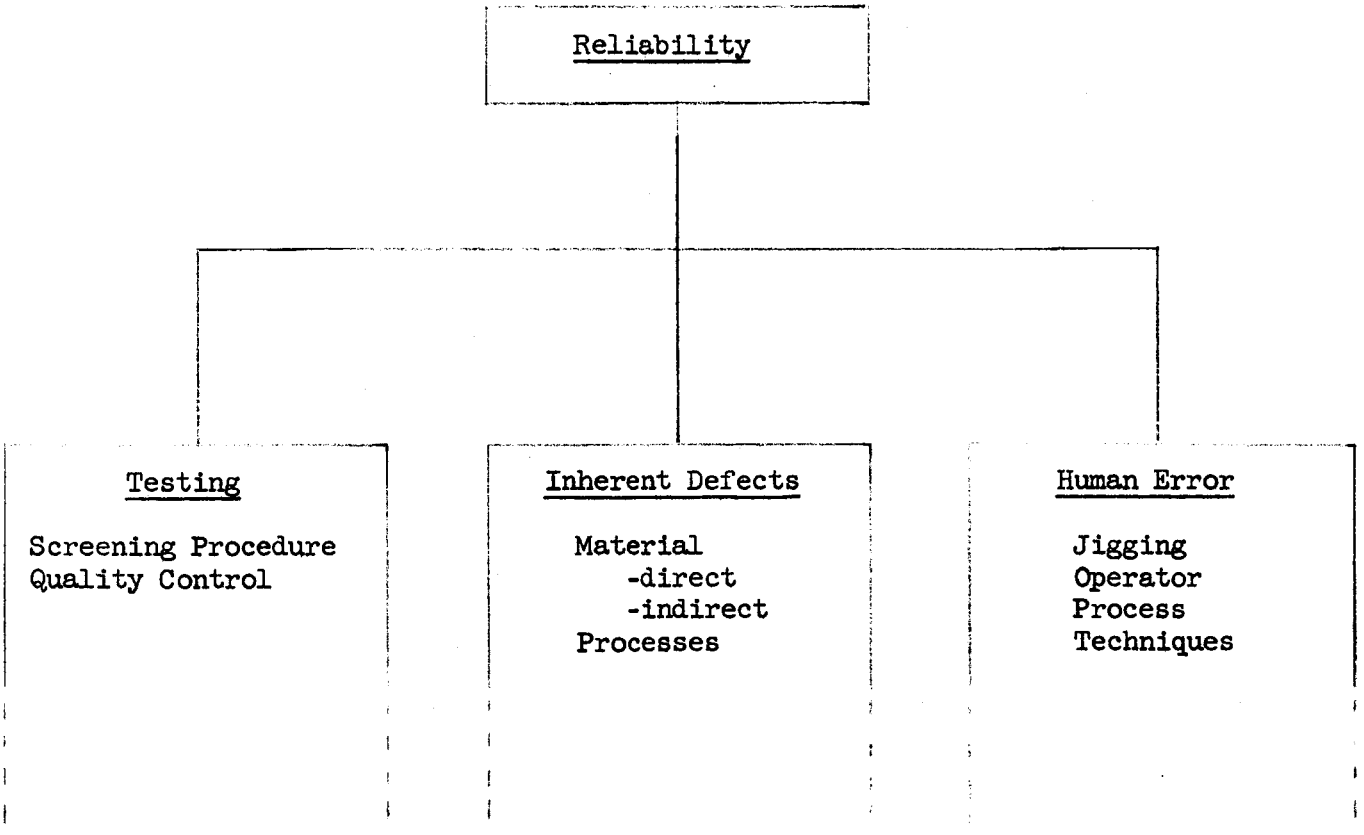

Reliability
Testing
Screening Procedure
Quality Control
Inherent Defects
Material
-direct
-indirect
Processes
Human Error
Jigging
Operator
Process
Techniques

Fig. 1

1. Degradation failure--a device which shows a change of > 20% from the initial reading on any parameter measured.

2. Catastrophic failure--a network or device which becomes inoperative or degrades sufficiently to cause definite circuit malfunction.

2) OUTLINE OF WORK

2.1) Objective of Contract

The objective of the contract was to conduct a study to expose the outstanding materials and fabrication problems affecting yield and reliability of silicon planar devices. These devices were to include integrated circuits, and power transistors with ratings up to 10 amps and 100 volts V_{ceo}.

The study was to include both direct and indirect materials involved in making these devices and all fabrication steps were to be considered from the growth of the silicon crystal to the final test and inspection of the finished device.

The aim of this report is to present a detailed analysis of materials and processing problems in each of the fabricating steps in order of occurrence and then a list, in decreasing order of importance with respect to yield and reliability of technical problems under separate transistor and integrated circuit categories.

2.2) Program of Analysis

During the period of the reliability and yield problem analysis, a study was made of planar type transistors and integrated circuit failure modes and in what percentages they occurred. The Research Laboratories in consultation with the Semiconductor Division and the Molecular Electronics Division used the facilities at each location to pinpoint the many problem areas in device fabrication.

2.2.1) Reliability Program

To furnish a general idea of the extent of information available, the various production divisions carry on a reliability and testing program to meet all requirements of military and NASA high reliability programs. All quality elements are complied with either by monitoring, or by direct responsibility of the specific effort. A single standard inspection approach is maintained in a rigid manner, from material purchasing through the entire manufacturing line, to product shipment with traceability of all parts to raw materials as required.

Facilities are set up to subject the device or circuit to extreme packaging and evaluation tests. For example, extended life tests of a dual Nand gate have been conducted over a period of more than two years and have yielded innumerable improvements in existing techniques.

Current quality assurance of components involve the high-stress testing of production integrated circuits and transistors. These high stress levels of typical environments include mechanical shock and centrifuge, temperature cycling and step-stress, as well as thermal

electrical storage conditions which are designed to create failures. Upon failure the discrepant devices are sent through a vigorous failure analysis to determine the failure mode, its cause and mechanism. Once isolated the cause of failure can then be determined, the feedback used to possibly correct the product design, process, controls, materials, operator techniques or equipment. Improvements are thus introduced into the production line in order to eliminate or reduce specific causes of failure. The following outline describes a typical procedure in more detail:

I. Information Input for Failure Analysis
   - A. Operational Field Equipment
   - B. Environmental Test
   - C. Accelerated Life Test
   - D. Electrical Screening
   - E. Step-Stress Tests
   - F. Special Customer Tests

II. Failure Analysis Procedures as Required
   - A. Failure Verification + Classification - (Electrical)
   - B. Outer Visual Inspection (Mechanical)
   - C. Hermeticity Test
   - D. X-ray
   - E. Lid Removal
   - F. Inspect and Photograph
   - G. Electrical Probe

H. Chemical Analysis

I. Sectioning

J. Special Studies

K. Data Analysis

L. Summary Report

After the isolation of the failure mechanism, a concerted effort is made to attribute the cause to one or more of the following reasons:

III. Cause of Failure

A. Product Design

B. Materials

C. Processes

D. Controls

E. Equipment

F. Operator Techniques

Once the cause of failure has been located suitable modifications can be made to the process to eliminate the problem.

2.2.2) Devices Analyzed

(a) Integrated Circuits

For the purpose of this report an integrated circuit will be defined as a solid circuit element into which more than one recognizable device has been fabricated and interconnected. These are types which are monolithic silicon in which all circuit and isolation elements are diffused in a silicon chip, and the interconnections and crossovers are formed by means of metal films deposited on the top of the passivating oxide.

Data from simple circuits of 6 output leads (3 transistors and 4 resistors) up to and including circuits containing 12 output leads (6 transistors, 10 diodes, 10 resistors and 2 capacitors) was analyzed for various failure mechanisms. The circuits which were scrutinized were those containing most of the common active and passive regions such as NPN and PNP transistors, diodes, resistors and capacitors. These particular devices have been fabricated by the following series of processes:

1. Epitaxial growth
2. Isolation Diffusion
3. Base and Resistor Diffusion
4. Emitter Diffusion
5. Contact Metallization
6. Bonding of Die to a Header for Encapsulation
7. Bonding of Wires from Silicon Die to Posts
8. Enclosure

From this point in the process, screening and acceptance tests were performed.

(b) Transistors

The processes involved in the fabrication of integrated circuits are in most cases common, also, to the fabrication of low and medium power planar transistors, except that the problem of interconnection leads does not arise for single devices. The major area of difference for high power transistors occurs in the region of assembly and

a reversible one in which rapid changes in concentration of doping compounds in the incoming gas stream are rapidly reflected in the doping level of the growing crystal. Contamination of the dopants is highly possible through etching of the silicon substrate before deposition.

Defects other than variation of impurity content which are found in epitaxial silicon include nonuniform thickness and crystal imperfections. Studies have shown[1] that the crystal imperfection of an epitaxial layer has a direct relation to the condition of the substrate onto which the material is grown. One of the often occurring imperfections found in these thin layers is that of a stacking fault which, although found in standard material, is primarily associated with epitaxial layers. This defect appears as a characteristic small triangle or line on the surface and propogates along one or more of the three inclined <111> planes. The initiation of the defect is usually attributed to unclean or oxidized substrate surface, this being either mechanical damage or contamination in the form of particles or thin films. P-N junctions in semiconductors containing stacking faults fail to exhibit anomalies which can be directly attributed to faulting, however, segregation of impurities may lead to disturbances in electrical parameters. Undesirable "soft" reverse characteristics of p-n junctions have been found to be the result of metallic precipitates occurring at these defects.[2]

b) Standard

In the manufacture of standard silicon bulk material,[3] most hyper-pure silicon (5×10^{13} atoms/cm^3) at present is made by the reduction of trichlorosilane by hydrogen according to the relation:

$$SiHCl_3 + H_2 \rightleftharpoons Si + 3HCl$$

The use of this method rather than the zinc reduction process used formerly has resulted in a decrease in impurity content by at least an order of magnitude. This has the consequent effect of improving the control of subsequent doping as well as improving the lifetime of the material.

The performance of most semiconductor devices to some extent depends on the bulk properties of the background material, the grain boundaries of polycrystalline material exhibiting different electrical properties from those of the bulk. In order to increase reliability and yield in both small areas and large area devices, a good low crystal imperfection bulk material must be used and it must be processed under conditions of contamination-free atmosphere and materials. Although defect-free crystal is never produced even by the most refined techniques, gross imperfections are to be avoided since they lead to variations in the diffusion or alloying characteristics. These effects as well as those doping non-uniformities produced by the precipitation of metals at dislocations cause leaky p-n junctions[2]. The most common ones are listed below:

(i) Dislocations

Crystal dislocations are produced by plastic deformation of hot crystals, nucleation by foreign particles, fluctuations in growth rate, and spatial fluctuations in solute concentrations.[4] These defects are usually revealed by selective etching and then take the form of small pointed bottom pits, triangular in shape, and formed at the interesection with the surface.

(ii) Twin Boundaries

A twinned crystal is a crystal in which the lattice is of two parts related to each other in orientation as mirror images across an interface called a twinning plane.

(iii) Slip

A planar slip in a crystal occurs due to plastic deformation in which one part of the crystal undergoes a shear displacement relative to another. The displacement takes place in a definite crystallographic direction and usually on a specific plane. The extent of deformation is traced through the crystal by the etch-pit method which in turn develops the motion of dislocations through the crystal.

(iv) Lineage

The surface over which a crystal is in contact with other crystals in a solid body is a grain boundary. Any point in this surface or interface constitutes the junction of at least two differently oriented crystal lattices. When the orientation is greater than one minute, it is defined as a large angle grain boundary developing from a line of dislocation etch pits with a linear density of 25 pits per mm.

Variations in resistivity also can lead to irregular electrical characteristics and non-planarity of diffused junctions. The effect has been found to be more serious in large area devices where high currents are usually found, since current crowding will occur at low resistivity regions. Variations in resistivity are due to the segregation of dopant at the freezing interface during crystal growth, volitalization of dopant from the molten region and melt turbulence.

In small area devices, since a large number of devices are made on a single wafer, variations in properties over the wafer result in variations in device characteristics. Whereas, these same variations would have an effect on individual device performance in large area devices.

Imperfections in crystal lattice complicate the fabrication of small area devices where junction spacing is critical. Variations in junction depth will greatly alter device performance especially in high frequency types. Usually devices made from lineage regions of a wafer will have a non-planar junction and unsatisfactory characteristics. For certain low-leakage devices and especially high frequency types, it is believed that an extremely high degree of crystal perfection is necessary.

In large area devices any great clustering of dislocations is to be avoided since temperature rise in these small regions of the device would be excessive.[3]

The active region of the larger power devices often occupies the entire crystal wafer for adequate dissipation of heat and restriction of current densities.

3.2) Oxide Growth

Silicon dioxide layers are generally grown on surfaces of an etched or polished slice for the purpose of subsequent diffusion by masking. At least three processes are in current use for growing such layers namely, anodic, pyrolytic and thermal oxidation.

(i) Anodic Oxidation

Oxidation of silicon by anodization is performed by arranging the silicon as the anode of an electrolytic cell containing a suitable conductive electrolyte. Oxygen anions formed in the cell react with the silicon to form silicon dioxide.

(ii) Pyrolytic Oxidation

Silicon dioxide is formed by the pyrolytic decomposition of tetraethyl othosilicate vapor at 600°C to 800°C. The silicon dioxide deposits on the silicon substrate as a fairly uniform layer.

(iii) Thermal Oxidation

Thermal oxidation of silicon is carried out by heating the silicon to a high temperature ($\sim$1100°C) in an oxidizing atmosphere of water vapor or oxygen.

The thermal oxide method has proven to be the most practical at the present for making planar silicon devices. The nature of this passivating surface achievable upon integrated circuits and transistors, to a great degree determines the level of performance and reliability that may be expected from these devices. Achieving a stable surface has

been essentially brought about by the thermally grown silicon dioxide which serves as a diffusion mask as well. Although silicon dioxide passivated devices do exhibit substantial stability, deterioration of device properties still can take place upon exposure to high humidity over long periods of time. Also, oxides subjected to high fields have been found to cause parameter drift or even catastrophic failure over extended periods.(5)

The processes used in the development of a device tends to complicate the problems of an already complex oxygen and silicon system. During these processes, oxides are subjected to both boron and phosphorus dopants as well as trace residues present from slice cutting, etching and polishing procedures. Contamination of the surface oxide may alter device performance either radically in a short time or gradually over a long period of time. The oxide over the surface of a device is really a multilayer structure of many oxides which have accumulated during each diffusion step. During and in between the various oxidation cycles, different impurities are present in the surrounding atmosphere as well as accessible from wet chemical processing and cleaning steps required during fabrication of the device. Contamination of this sort usually evidences itself as junction leakage or channeling.

Aside from junction passivation and the protection against the diffusion of doping atoms, the oxide must also insulate surface conductors from the silicon. Voids in the oxide layer due to either non-homogeneous structure or faulty processing have been found to be a very serious

problem in yield and reliability especially with integrated circuits. If the hole in the oxide exposes a junction or permits contamination to reach the silicon layer, the result will be either catastrophic failure or a long term drift of device parameters. An added hazard presented in integrated structures comes about if the oxide void happens to be in the path of a surface interconnection. In this instance an interconnect to substrate short will occur either during the following process steps or during application of the device. Voids, other than those produced by defective processes, are often found to be caused by impure or damaged silicon which generates imperfect structure in the oxide during growth.

The imperfection of oxide layers has been studied by both transmission and replica electron microscopy and also by treatment of slices at high temperature by chlorine etch methods.(6) Figure 2 shows a transmission electron micrograph of an oxide layer formed on a silicon slice. The spots marked A are from abrasive particles and B from dirt. Areas C are believed to come from relatively deep pits. Since the oxide follows the contour of the surface, there would be an oxide "dimple" after the silicon has been removed. The transmission electron diffraction patterns showed a spot pattern characteristic of abrasive particles superimposed on a very weak diffuse ring pattern characteristic of amorphous material.

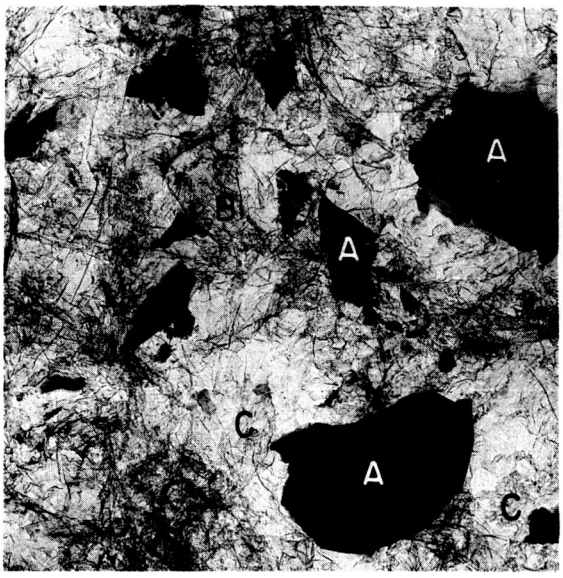
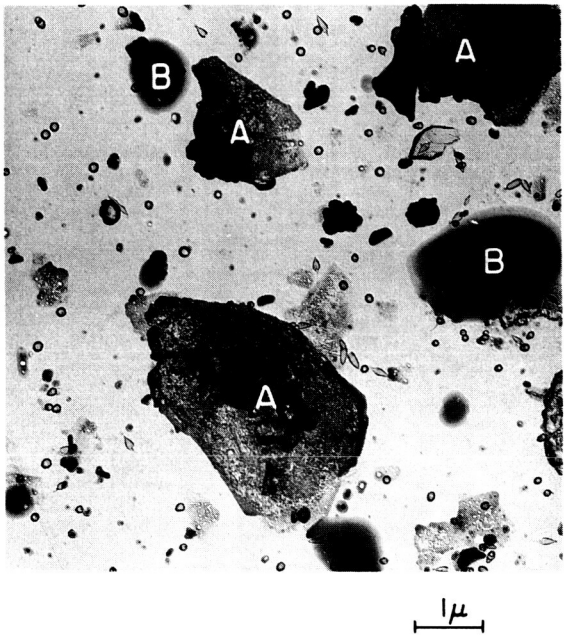


Fig. 2 –Transmission electron micrograph of oxide layer produced during abrasion with 600 mesh alundum slurry
A: Abrasive particle B: "Dirt" C: Folded pit



Transmission electron micrograph of oxide layer produced by etching in CP4 for 5 min
A: Abrasive particle B: "Dirt"

3.3) Mask Making and Photolithography

(a) Mask Making

A set of fabrication masks, through the use of which many of the processes utilized are made to give patterned geometries, is basic to any planar device. In the development of a suitable set of masks, an accurate large scale layout is first made and undergoes photographic reduction. Repetition is then made on a high resolution plate to give a multiplicity of patterns covering approximately 1" area of the emulsion.

Producing masks with these emulsions free of defects is extremely difficult, the problem being accentuated when the active areas of the complete unit become progressively larger. Besides the defects produced in the emulsions during mask fabrication, this soft emulsion is also highly susceptible to damage from the surface of processed materials or from jigs and fixtures of other processes. This results in masks that may be used for only a limited number of times. Furthermore, the life of these masks is also limited by breakage and sticking of photoresist which alters the patterns locally.

A more rugged mask is the metal film on glass, patterned photolithographically using an emulsion master. The metal film on glass mask can be scrubbed for cleaning and does not scratch easily. It is however much more expensive than the emulsion type, since its fabrication requires more elaborate processes and the yield of good masks is low. However, the contrast between clear and opaque areas is much sharper than can be obtained with an emulsion mask.

Masks containing spurious spots in the emulsion are indirectly responsible for low metallization and diffusion yield and for a serious reduction in reliability of the finished device. These defective masks, when used in conjunction with standard photoresists, permit etching in unwanted regions and inadvertant removal of oxide in regions not desired. This then leads to diffusion spiking and shorts of interconnects through to the substrate regions.

(b) Photolithography

Patterns in the oxide for localized diffusion into a silicon wafer are produced by spinning a thin layer of photosensitive emulsion on the oxide and exposing the pattern by means of an ultraviolet-rich light source through a contacting mask. Subsequent processing entails developing, washing away the regions masked from the light, then baking to harden the resist. Patterns nearly as fine as those that can be reproduced in a mask can be etching in the oxide layer, which under ideal conditions can be as small as 2 microns.

The many photoresist steps that a wafer undergoes before it is completed probably account for the greatest loss in yield of any process. First, the photoresist contains polymer aggregates or other particles that give rise to pin holes and poor edge definition. Some of these particles can be removed by filtering, but this filtering operation is limited by the level of viscosity that must be maintained. The results of the resolution and masking capabilities of some standard photoresists are shown in Tables I and II. Table I shows resolution results with

respect to dilution of the resist. Table II shows the yield of a number of devices on slices going through all processes (etching, diffusion), however, no masks were used so that the masking capabilities of the resists only could be examined. The results of these tests show that a resist that gives good oxide protection is limited in resolution qualities and vice versa.

The adherence of all standard photoresists is governed, to a great extent, by the condition of the silicon surface as well as by the resist application procedure. In the first case when moisture or solvents are retained by the oxide, subsequent temperature cycles tend to drive these residues off to the extent of lifting the resist from the silicon surface. In the latter case, optimum application procedures such as spinning speed, ambient and baking cycles are still widely determined by "rule of thumb" methods.

In cases where the resist does adhere well, if etching of the oxide is carried out for too long a period of time, undercutting can occur. Undercutting is also a problem when it is required to etch through oxide layers of different diffusions which normally have different etch rates and are of different thicknesses. In this respect, integrated circuits suffer a greater loss in yield than small single transistors, since a more complex pattern must be treated to the same photoresist steps without the appearance of a serious flaw. Also, transistors are not subject to the evaporated lead problems of integrated circuits.

TABLE I

RESOLUTION TESTS

Resist Solution (Parts by Volume)	Resolution as Determined By Mask Design (Lines/mm)
Undiluted Kodak Metal Etch Resist	40 - 60
10 Parts KMER 1 Part KMER Thinner	50 - 70
4 Parts KMER 1 Part KMER Thinner	80 - 90
2 Parts KMER 1 Part KMER Thinner	90 - 100
4 Parts KMER 3 Parts KMER Thinner	120 - 140
1 Part KMER 1 Part KMER	160 - 180
Undiluted Kodak Photoresist	200 +

Mask Design	Positive Mask Measured Line Width	Positive Mask Measured Line Separation
200 Lines/mm	.085 mm	.106 mm
180 Lines/mm	.100	.117
160 Lines/mm	.112	.135
140 Lines/mm	.120	.152
120 Lines/mm	.140	.168
100 Lines/mm	.190	.209
90 Lines/mm	.214	.219
80 Lines/mm	.236	.248
70 Lines/mm	.268	.271

TABLE II

Oxide Masking Tests

Resist Solution	Units Tested	Yield
2,500 - 3,500 A°		
Undiluted KMER	101	60.5%
10 Parts KMER 1 Part KMER Thinner	32	50%
4 Parts KMER 1 Part KMER Thinner	31	45.5%
2 Parts KMER 1 Part KMER Thinner	157	47.2%
5 Parts KMER 3 Parts KMER Thinner	31	19.3%
4 Parts KMER 3 Parts KMER Thinner	34	8.2%
1 Part KMER 1 Part KMER Thinner	68	1.5%
Undiluted KPR	50	0%
No Photoresist (Group 2)	225	87%
6,000 - 7,000 A°		
Undiluted KMER	96	86.4%
10 Parts KMER 1 Part KMER Thinner	32	84.2%
4 Parts KMER 1 Part KMER Thinner	35	82.7%
2 Parts KMER 1 Part KMER Thinner	159	78.3%
5 Parts KMER 3 Parts KMER Thinner	32	40.6%
4 Parts KMER 3 Parts KMER Thinner	33	15.5%
1 Part KMER 1 Part KMER Thinner	65	1.5%
Undiluted KPR	36	8.3%
No Photoresist (Group 2)	103	99.2%

Lastly, the residues left over from these resist processes as well as particles of the resist itself, can act as deleterious contaminants in the succeeding diffusion operations.

3.4) Diffusion

The diffusion of an impurity into silicon constitutes a large part of the processing that a silicon wafer undergoes on its way to yield a planar transistor or an integrated circuit. Phosphorus and boron are the two most commonly used impurities to form base and emitter regions of transistors and integrated circuits. Basically, diffusion consists of heating silicon wafer to a temperature at which the impurity diffusion coefficient is reasonably large, and passing a vapor of the impurity, diluted in a carrier gas, over the silicon to form active regions. In some cases, a thin oxide layer is grown which, due to the presence of the impurity vapor, is heavily doped with the impurity. This impurity source in the oxide then acts during a subsequent heat cycle to diffuse into the silicon at a reasonably controllable rate.

Defects originating in the diffusion process are due to improper impurity control, contamination, or microplasmas in material that has been chemically polished. This fact is borne out even more by the results of studies which have shown that damage as deep at 10 microns is produced by standard mechanical polishing.(7)

Investigations by others(8) have shown that a strong influence on microplasmas is exerted by dislocations, since diffusions are enhanced along these material imperfections resulting in weak spots in the base

layer.[7] Studies show that if there are no dislocations in the base layer region, the boundary of the collector-base junction is the next most favored location for light emitting regions.

Some units that had reasonable collector-base breakdown voltages after boron diffusion, developed microplasmas during subsequent phosphorus diffusion and displayed deteriorated junction characteristics upon analysis. These were probably due to diffusion spikes caused by holes etched in oxides in photoresist steps prior to diffusion.

The most convincing data that donor contamination is the primary cause of this phenomena is shown by the following findings:

1. The application of spark mass spectrographical analysis of the light emitting regions indicate traces of phosphorus present, being introduced before initial oxidation as well as during boron diffusion. The results of the spectrographical analysis is shown below:

Sample #	Chlorine ppm	Sulfur	Cr.	Phos.
2-25	500	100	1	1
2-2	---	---	5	1
1-8	---	---	-	1

2. Angle lapping and staining of isolated light emitting regions indicate the presence of phosphorus diffused pipes. This can be seen in the microphotograph shown in Figure 3.[7]

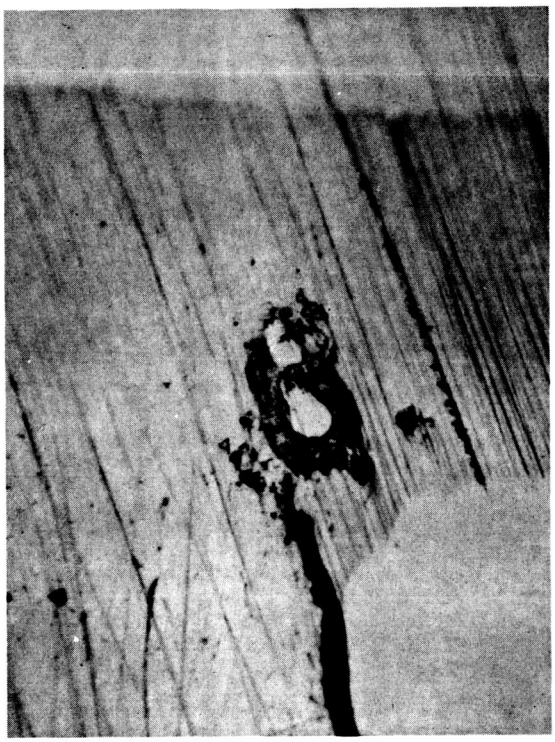


Fig. 3 - N-Type Contaminated Region in
P Diffused Area Revealed by Angle Lap
and Stain

3.5) Metallization and Lead Attachment

3.5.1) Low Power Devices

For low power transistors and integrated circuits, ohmic contacts to diffused regions and interconnection of circuit elements are accomplished by a metal evaporation and photoresist patterning scheme. Evaporated thin layers of aluminum are almost always used, because it adheres well to the silicon dioxide, will universally form "non-injecting" type ohmic contacts to heavily doped n and p regions and is compatible with evaporation and photolithographic etch processes. Crossovers from component to component are also made quite easily with aluminum, providing good adhesion properties and low resistance paths.

The vacuum deposition of aluminum is accomplished by the transport of the metal from a heated evaporation source to a surface, in a vacuum of 10^{-5} torr or lower. At these pressures the mean-free-path of the evaporated molecules or atoms exceeds the chamber dimensions sufficiently so that they travel essentially in a straight line between the source and substrate.

Of the many metals possible for use, aluminum gives one of the highest bond strengths when bonded to any other metal.[8] Gold, with high chemical stability, is the most frequently used material for thermo-compression or "nail-head" bonding, in the connection of bonds between package leads and metallization at the die.

Thermocompression bonding or "nail-head" bonding is the joining together of solid materials to each other by the application of heat and pressure for a given period of time to create plastic deformation and intimate contact between the solids. Standard thermocompression and "nail-head" bonding equipment contains, the usuals pressure device in the form of a wedge or hollow tip, a heating mechanism, a method for maintaining the "work" in an inert atmosphere, and various mechanical arrangements to facilitate positioning and operation of the bonder.

Various deposition parameters influence the physical properties of the deposited films and care must be taken to maintain proper control in order to obtain reproducible results. The most important of these properties are: chamber pressure, purity of ambient, source and purity, source to substrate geometry, evaporation rate, substrate temperature, film thickness and composition.

Photoresist techniques used in negative removal of the aluminum to form the actual pads for ohmic contacts and leads of the interconnection pattern present ovbious defects in the metallization system. These have been analyzed in the section on oxides and photoresist.

In the placement of gold bonds on aluminum, the process is extremely critical in requiring ultracleanliness, fully annealed wire and precise operating conditions. The proper inert atmosphere may contribute to reproducibility and reliability by reducing contamination during heating. To produce bonds of high strength and low variability, the material shoud be at a temperature in the plastic deformation range.

An important factor in the bond between any two materials is the effective area of contact as contrasted to the "apparent" area of contact. Equally important is the requirement that the ohmic contact needs mechanical support and a good thermal path.

When considering the overall system the major disadvantages of the aluminum-gold system are:

1. The formation of a ternary $AuAl_2$ complex which promotes the weakening of a bond to the point of occurrence of opens by shock and vibration. This formation is accelerated by exposure to higher temperatures even for short intervals.

2. The softness of the aluminum which leads to inadvertant scratching open of interconnections by masks, probes or jigs which must contact the surface of the die during subsequent processing.

3. The reaction of aluminum with water vapor to produce the decomposition of the interconnections and contacts.

4. The poor mechanical bond occurring when aluminum does not adhere well to the SiO_2 surface or when a poor gold-aluminum junction is made.

Some efforts have been made to circumvent these problems. The use of aluminum instead of gold wires avoids the problem of bond weakening due to alloy formation at the contact but the lead strength, due to the softness of the aluminum and the aluminum-water vapor reaction and interconnect damage problems are still present.

The substitution of other metals for aluminum in the contact and lead materials again leads to problems of bond strength and possible alloy instability.

3.5.2) High Power Devices

In the case of larger devices where current handling capacity and power dissipation is important. The use of thin bonded leads is not desirable. For these devices the normal practice is to metallize the contact areas either by evaporation or by electro plating and then to solder conductive contacts (or tabs) to these regions. One of the contacts, normally the collector, usually serves also as a heat sink and forms part of the encapsulation.

The soldering operation usually involves the use of some type of metal preform which is placed between the contact area and the tab. The assembly is then heated and the metal preform melts and forms the solder bond from tab to contact area.

The problem arises here of ensuring a good thermal and electrical contact in the solder joint. Poor contacts can cause localized overheating and failure of devices. The problem is further complicated by the need to create a good thermal expansion match between the silicon and the tab. Thermal expansion mismatch can cause cracking of the silicon when the device is dissipating power. This problem also occurs in the mounting process.

3.6 Encapsulation

3.6.1 Mounting

The attachment of a transistor element wafer to a supporting header or post must be designed to provide proper mechanical support and good thermal and electrical connections. The dice is obtained when individual chips or circuits are separated from the parent wafer by means of scribing with a hard pointed tool and breaking apart. This operation is much like diamond cleaving; the pattern must be initially oriented on the wafer in such a way that cleavage occurs along favorable crystallographic planes. The individual dice are then bonded to a package by glassing (pyro-ceram) or metal alloying techniques.

Glassing isolates the silicon from the package; metal alloying electrically connects the two unless a metallized ceramic is used in the package. The bonding techniques available for this operation are:

1. Alloying by manual scrubbing.
2. Alloying by ultrasonic scrubbing.
3. Alloying aided by deposited films.

Various alloys liquefying in the 400°C to 600°C range have been mainly used but the most common have been the eutectic alloys fo gold-silicon or gold-germanium. These solder preforms when placed between the silicon and gold-plated kovar or molybdenum header, provide an excellent bond at the silicon-gold eutectic temperature.

Alloying by scrubbing, the technique in most common use at present for performing the above operation, serves to break down the brittle oxides formed by the semiconductor. This operation entails holding the dice by some rigid fixture directly on top of the header or preform and scrubbing the dice with light pressure in a nitrogen atmosphere. The eutectic alloy is formed and a bond occurs on cooling.

The mounting process must be one which will not damage the element or device nor introduce adverse contaminants. Stress conditions, sharp changes in wafer cross section, surface scratches or notches, voids or inclusions in the alloying layers and excessive process temperatures are all detrimental to the final characteristics of a semiconductor device. Where scrubbing techniques are used, disadvantages lie in the operator dependence of the process; many types of defects result from limited skill or carelessness. This problem is somewhat alleviated by ultrasonic scrubbing methods, however, many bonds are still defective from uneven eutectic formation and fillets. Another serious bonding defect is that of thermal fatigue which often results from the sequence of thermal cycling, plastic deformation and recrystallization of solders used in the alloy.(9) This condition limits power dissipation, causes localized heating or hot-spots and eventual failure of the device. Harder solders do reduce this problem but also enhance fracturing of the silicon when thermal expansions are not matched.

3.6.2) Package Sealing

The device or circuit encapsulation process must be one which fulfills the following requirements:

1. Protect transistor or integrated circuit elements from mechanical damage and changes in the external environment.

2. Provide external terminations for device leads.

3. Permit heat dissipation from the device.

Several kinds of encapsulations, in a variety of sizes, are now utilized for transistors and integrated circuits. Three of the most common types in use today are the standard and multi-lead transistor metal-glass package and the integrated circuit flat package.

The three most common methods of sealing these packages are:

1. Resistance welding.

2. Cold welding.

3. Soldering.

The most widely used method for closing metal-glass packages is resistance welding. This consists essentially of obtaining a line contact between header and cap and pulsing a large amount of current through the assembly at the point of contact. Simultaneously, pressure is applied to force the heated metals together.

Cold welding, which has some advantage over resistance welding, is a type of pressure welding in which the metals to be joined are deformed by 65 to 95% at room temperature.[9] Protected or cleaned copper is the usual metal employed in this process.

Lid soldering is used primarily on flat packages, the operation consisting simply of the soldering of a gold-plated kovar lid to the rim of a flat package in a nitrogen or hydrogen furnace at approximately 320°C.

Welding by resistance technique is both reliable and economical, however, the process does have a number of problems associated with it. These are:

1. Weld flash may contaminate the device during welding.

2. The device may be affected by gas desorption from the can wall.

3. Excessive heating during welding may become injurious to large devices or cause inversion of oxide layers to produce leakages at device junctions.

4. Electrode care presents many problems during production. Although cold welding corrects many of these problems it suffers from the following disadvantages:

1. The use of copper places some restrictions on many applications.

2. There are also indications that certain imperfections in the weld cannot be detected until after an excessively long aging period. Certain organic materials present in submicroscopic quantities contribute originally to making a bond deteriorate with time and establish a defective hermetic seal.

3. The need for ultracleanliness.

4. The need for high quality gold plating.

5. The need for extremely high pressures.

Soldering is more suitable where good electrical contact cannot be made to the seal however the following problems are still present:

1. The device may be affected by gas desorption from the can wall or contamination from the solder.

2. Excessive heating during soldering may become injurious to large devices or cause inversion of oxide layers to produce leakage at device junctions.

3. It is necessary to have high quality gold plating and ultracleanliness to affect a good seal.

The effectivenss of the seal is checked by a combination of a helium mass spectrometer leak test for small leaks and a bubble test for gross leaks. The bubble test is however not adequate to cover the range of leaks down to the region served by the helium leak test.

3.7) Quality Demonstration Testing

At the point of encapsulation when a hermetic enclosure is sealed about a device, fabrication processing is completed and only testing and screening operations may be performed. The purposes of the testing and screening operations are twofold:

1. To insure that all (or a certain percentage with a statistical confidence factor) of the devices shipped to customers meet agreed-upon performance specifications at time of shipment.

2. To attempt to insure, using the latest techniques and information, that any weak devices introduced by faulty design of fabrication processing are made to fail by normally nondestructive environmental stressing and are detected and removed by the final electrical performance screen.

To state these more concisely, the first purpose is motivated by an insistence on quality performance of each device when shipped, and the second on a desire for the highest reliability of device performance when used in a realizable system in the future.

The sequence of tests and screens may vary depending upon the device, the demands of the customer, and economic considerations, but in general the following types of tests and screen are included at some point:

a.) Production Final Electrical Test - All devices are subjected to a guard-banded series of electrical performance tests which in general include only a sufficient number of all performance parameters to enable the vendor to guarantee his entire performance specification.

b.) Environmental Stress - All devices are subjected to a sequence of environmental stresses which might include but is not limited to the following:

(1) High temperature stabilization bake.

(2) Centrifuge.

(3) Temperature cycling.

(4) Thermal shock.

(5) Mechanical shock.

(6) Vibration (operating and non-operating).

The stresses chosen for these tests are generally those to which the devices will be exposed in system operation, and the stress levels chosen are to be nondestructive for a reliable device.

The purpose of these tests is to cause potentially unreliable devices to either degrade or fail catastrophically in the vendor's plant and subsequently be screened out by electrical performance tests.

c. Burn-In - Some failure mechanisms are excited only by the presence of localized electric fields and heat distributions which result when normal operating biases are applied to the device. In order to conduct a worse case test, burn-in is usually performed under normal operating biases at the highest operating ambient permissable. The purpose of this test is again to cause either degradation or catastrophic failure of potentially unreliable devices. Those which fail are then screened out at subsequent electrical performance screens.

When the aforementioned series of environmental, thermal, and electrical stresses has been completed and all failures whether degradation or catastrophic have been removed by electrical screening, all devices of the lot screened should be capable of performance to the stated specification and as such should be acceptable for shipment to the customer.

In some cases, however, the customer desires additional assurance that all parts do indeed meet the performance specification, and he requires that a sample of devices be pulled from the parent lot using statistically determined sample sizes for the degree of

assurance desired. This sample is then subjected to a series of Lot Acceptance Tests similar to those of Sections b - c described earlier. Customer acceptance of the lot is then contingent on the successful outcome of the series of lot acceptance tests. Because the stress levels chosen for these tests are supposedly non-destructive to reliable devices, failures in the lot acceptance test sample which was selected from a lot of good, tested devices may be grounds for lot rejection, depending upon the nature of the failure.

A summary of some of the problems of this cycle of testing and screening and their relationship to device reliability and yield is as follows:

1. The test sequence is overly complicated and expensive. In some cases tests are duplicated resulting in wasted money which could be spent elsewhere to improve yield or reliability, or resulting in products which are not as reliable as desired.

2. The crossover points where stress levels turn from non-destructive to destructive are not well known for all stresses used. In some cases, a test which is performed to weed out potentially unreliable devices may in reality be weakening a device which before the test was reliable.

3. The effects of some environmental stresses may be cumulative, and in the process of subjecting devices to repeated nondestructive stresses, the cumulative effect may be destructive. The same problem as occurs in (2) above may be taking place.

4. In many cases, the series of environmental tests chosen bears no relationship to the anticipated environmental stresses anticipated in systems use. This happens either because the stresses to be encountered are not known, or because of some idealistic desires to have the most stress resistant device obtainable without regard to its end use. Considerable money and overstress could be saved by a more judicious choice of stresses and stress levels.

5. The combination of some nondestructive environmental stress tests followed by lot sampling is a procedure carried over from earlier transistor and diode manufacture where the levels of reliability were not as high as those expected for integrated circuits and planar power devices. This sequence should be thoroughly examined to see if it does what it is intended to do in the way of guaranteeing high reliability products to the customer at a reasonable price or whether some modification should be made.

3.8) Reliability Characterization

Classical component reliability characterization is statistically based wherein a large number of manufactured parts is defined as a population which is then characterized by a failure distribution function. With a knowledge of the form and parameters of this function, probabilistic statements concerning the reliability of a system fabricated from such parts may be made using mathematical statistics. In general, this technique requires a large initial experiment to determine the form of the failure distribution function, as well as smaller periodic tests to verify the values of the parameters of the distribution function.

Used in the past and still in use is the large-scale operating life test technique for the generation of a number which represents average failure rate or mean-time-to-failure of a functional electronic block. Present industry figures for the failure rate of a circuit as complex as a single logic gate range from .05% per 1000 hours to .005% per 1000 hours.

Although theoretically there is no reason why this technique may not be used to characterize integrated circuits, practical problems arise which severely limit its ability to produce useful information. A discussion of these problems is provided in the following paragraphs.

3.8.1) Failure Distribution Function

Before any characterization of reliability may be made, the form of the failure distribution function, which portrays number of failures as a function of time, must be determined and a mathematical functional expression of this form must be available. The form of this function has not been determined for integrated circuits, and because of economic considerations, it will in all probability be a long time before it is found. The three types of failure distribution functions found to be useful for discrete component characterization are the Exponential, the Lognormal, and the Weibull distributions. The Exponential distribution is a random failure distribution, and because of its mathematical simplicity, it is generally assumed when a distribution is needed and no data is available. The Lognormal distribution is a

variation of the standard Normal distribution often found and has been successfully applied as a diode failure distribution function. The Weibull distribution is more general than the other two possessing shape parameters which allow for a wide variation of functional shape, and it has been successfully applied as a failure distribution function for certain high reliability transistor. Because a demonstration of the proper failure distribution function for integrated circuits has not been made, arbitrary assumptions of applicable functions are made depending on the experience of the one making the assumption.

3.8.2) Step-Stress Testing

In its most general form, Step-Stress Testing should provide a means to relate short-time, high-stress tests to long-time, operating-ambient conditions thereby providing a quick assessment of reliability. Implicit in the use of this technique, however, is the assumption of a Lognormal failure distribution function which is entirely arbitrary at this time. Independent of this problem, Step-Stress Testing has value in providing a quick comparison of the resistance of two or more groups of parts to thermal stress.

3.8.3) Exponential Distribution

If an arbitrary assumption of a failure distribution function is required, the Exponential is generally the one assumed. The economic difficulties of demonstrating a mean-time-to-failure with high confidence are illustrated by the following example. In order to demonstrate a failure rate of 0.0001% per 1000 hours with 90% confidence,

an operating ambient life test including 23,000 functional blocks would have to operate 11 years with no failures. Such an experiment would run in the hundreds of thousands of dollars and would demonstrate the required failure rate for only one functional block. The cost of such a test coupled with the fact that it would provide information about only one of the roughly one hundred integrated circuit designs now developed makes such a venture unrealistic. This conclusion is further underscored by the 11-year time period required for completion of the experiment in a time when systems become obsolete in a matter of several years.

3.8.4) Proof Tests

The economics of proving attainment of a goal failure rate will soon make such tests unworthy of consideration as a test performed by a vendor on his components. The previous example provided an illustration of such a test for the Exponential Distribution, and similar considerations apply to the other two. The present practice by the military systems customers of purchasing only a limited number of systems requiring small volumes of several types of functional blocks further supports this conclusion.

Several alternatives exist as solutions to this problem. From the customer's standpoint, he may obtain reliability information about a vendor's parts from the experience he has with the systems he makes. This technique does not help the vendor, however, because the time delay

of information feedback is too great. The vendor's alternative is to go back to the thing which is common to all blocks he makes--his processing. The role of processing in reliability will be discussed further in subsequent sections.

The discussion in this section has presented arguments to show that although not theoretically incorrect, standard component reliability techniques do not do his required job of providing useful reliability characterization data economically and in a timely manner.

4) CONCLUSION

4.1) Assessment of Factors

The relative weighting of factors contributing to loss of yield and reliability is difficult for two reasons. Firstly, it is strongly dependent on which combination of processes is used to fabricate each particular device and it would be necessary to integrate these individual weightings for the whole field of manufacture. Secondly, the level of technical achievement in different areas and therefore the relative importance of each factor would differ for each manufacturer. However, it is apparent that a more generalized list of problem areas can be drawn up in decreasing order of importance. Separate lists are presented for integrated circuits, low power transistors and high power transistors.

4.1.1) Integrated Circuits (Table III)

The most obvious problem area at present is in the package. This may partly be due to masking of less obvious defects by package faults. The problem does not seem so acute when a normal transistor

package is used instead of the flat package but in a considerable number of cases the flat package is necessary due to consideration of high density of circuitry. It is apparent that a considerable investigation of the package concept would be desirable. It is evident that package reliability is closely related to the size of the package, since the smaller geometries require a close tolerance on dimensions. The method of handling the package during testing and the process of mounting the unit into the electrical subsystem (e.g., printed circuit board) can also affect the reliability of the package.

It is also apparent that a more effective method of testing the hermeticity of the package would be desirable.

Wire bonds and interconnections form the next group of significant faults and again this may be because these defects can be observed readily in failed units. Problems in this area are mechanical or arise from interactions between the various metals and between the metals and silicon dioxide. A more detailed analysis of the mechanisms involved in these diffusion limited processes would lead to a better understanding of the significance of these factors in reliability. A redesign of the package which eliminated the need for bonds and wires would overcome the mechanical problems.

The dominant remaining failure modes are those factors that are primarily the result of bulk effects, which are often masked by the present high density of mechanical failures. These bulk failure modes are those effects which usually occur gradually over extended

periods of time as contrasted with mechanical failures (package, bonds, interconnects) which generally are of the catastrophic type. It is in these areas that investigation of improvements should be made, since mechanical problems, which are visible and more easily definable, can be solved by the present P.E.M. and M.M. investigations.

One of the remaining problems, especially the investigation of bulk effects, lies in the need for suitable non-destructive methods for exposing underlying defects. Techniques are available at present such as, Infrared Scanning, X-Ray Microprobe Analysis, Noise Measurements, Discriminant Testing, and Scanning Electron Microscopy.

Infrared scanning of a working device may indicate any hot spots which could lead to early failure. Noise measurements and discriminant testing allow significant variations from the normal unit to be investigated very thoroughly. X-ray microprobe analysis is useful for failure analysis to indicate any anomolous distribution of metals on the surface of the failed device. The scanning electron microscope is being used in failure analysis, since it is possible to detect areas of different surface potential. Inversion layers, anomolous diffusion regions and irregular depletion areas have all been detected with this instrument.

Problems associated with reliability improvement of the whole range of planar devices, now available, demand solutions. Since most of these devices will involve similar processing but different

maskings, a suitable solution may result which will be applicable to all designs, for factors pertaining to such design limitations as loading, lead parasitics, power dissipation, etc. Before such a system can be adopted, however, considerable evidence must be generated both in failure mode identification and test data to support its validity.

4.1.2) Low and Medium Power Transistors (Table IV)

As can be seen from this table the problems associated with these devices are very similar to those for integrated circuits. The exceptions are that the packaging problem is not so acute and also of course that problems involving interconnecting leads do not appear. It is apparent however that factors leading to improved realiability will be common to both groups of devices.

4.1.3) High Power Transistors (Table V)

The major problem area for the fabrication of reliable planar power transistors appears to be in the formation of a good electrical and thermal contact between the silicon and the metal mounting tabs. Good electrical and thermal characteristics are not necessarily independent of one another; from a device fabrication standpoint they may be considered as always interdependent. Poor thermal contact invites power dissipation problems and poor electrical characteristics. Faulty contacts by themselves may be responsible for power dissipation problems which would otherwise not be present.

A higher degree of process control during packaging appears to be quite important. High electrical leakage due to undesirable impurities present during the sealing operation, or at least finding their way into the package at this stage, indicates that more process control is wanting here. Poor sealing will obviously lead to high electrical leakage and can be overcome by improving the control on the package sealing process.

Surface electrical leakage due to imperfect passivating layers is a pressing problem. New or improved methods of producing uniform and stable pssivating layers--be they oxides or other materials--should be investigated. The absence of surface conversion as well as low electrical leakage should be the prime objectives of these new and improved methods.

The remaining areas are again similar to those discussed for integrated circuits and can be considered as a need to improve the quality of materials or processes.

TABLE III

INTEGRATED CIRCUITS

RELIABILITY FACTORS	ORDER OF IMPORTANCE	FAILURE MECHANISM	SUGGESTED REMEDY
Flat Package	1	Hermeticity Plating Thickness Variation in glass seal thickness	Correct present package Consider new high density package concept Improve package handling methods.
Wire Bonds	2	Plague formation or poor bond strength Wires touching lid or die Gold plating	Improved compatible metal system Different method of attaching package leads to die eliminating wires
Interconnections	3	Scratched aluminum Aluminum deterioration Opens at oxide step	Improved compatible metal system Protective coating of interconnections Improved evaporation techniques
Oxides	4	Pinholing Cracks Low dielectric strength Contamination and inversion	Non-porous photoresist Improved oxide growing and defect detection techniques Extensive surface studies
Circuit Design	5	Specification limits	New design or new specification limit
Testing	6	Transients and overloads due to incorrect testing	Better corrdination of user and manufacturer test methods.
Contacts (High Resistance)	7	Poor alloy Improper window mask dimension Incomplete oxide removal Misalignment	Improved alloying technique
Die Bonds	8	Cracked Silicon	Improved mounting technique
Junctions	9	Diffusion spiking	Nonporous photoresist Grow cleaner oxides

TABLE IV

LOW AND MEDIUM POWER TRANSISTORS

RELIABILITY FACTORS	ORDER OF IMPORTANCE	FAILURE MECHANISM	SUGGESTED REMEDY
Wire Bonds	1	Plague Formation or poor bond strength Lifting Aluminum Wires touching die	Change in metal system Different method of attaching leads to die
Oxides	2	Pinholing Contamination and inversion Cracks	Nonporous photoresist Improved oxide growing and defect detection Extensive surface studies
Junctions	3	Diffusion spiking	Nonporous photoresist Grow cleaner oxides
Contact (High Resistance)	4	Poor Alloy Improper window mask dimension Incomplete oxide removal Misalignment	Better registration methods Improved alloying techniques
Post Welds	5	Dirty wire or post Faulty technique (heat or pressure)	Different method of attaching leads to die
Die Bonds	6	Cracked silicon	Improve mounting technique

TABLE V

HIGH POWER TRANSISTORS

RELIABILITY FACTOR	ORDER OF IMPORTANCE	FAILURE MECHANISM	SUGGESTED REMEDY
Assembly	1	Localized overheating at contacts Cracked wafers Open circuit contacts	Improved methods for controlled joining of metal contacts to silicon dice
Package	2	High electrical leakage Contamination Poor sealing	Increase control on package sealing
Oxides	3	Surface leakage	Method for producing stable passivated oxides
Junctions	4	Current crowding due to microplasma breakdown or non-uniform diffusions	Investigate methods for producing more uniform oxides and diffused layers
Photoresist	5	Localized short circuits Diffusion defects	Increased control of photoresist processing

4.2) Recommendations

It is evident that the major problems affecting yield and reliability for planar device structures at the present time are in the areas of assembly and encapsulation. A new packaging concept for integrated circuits involving the encapsulation of subsystems and/or a new method of hermetic enclosure would contribute towards improved system reliability. However most of the other problems of assembly and encapsulation are mechanical in nature and are being vigorously persued in Production Engineering Measure and Manufacturing Method programs. Once these factors have been eliminated there will still remain the problems connected with inherent defects. These are features due to inhomogenuity of materials or faulty junction and oxide formation.

It is necessary that a rigorous program of failure analysis be carried out so that the significant defects related to failure and the mechanisms of failure may be recognized.

Using this knowledge an examination of the semiconductor material should be carried out at each stage of manufacture, to observe where and when the defects related to failure are introduced.

This program would then allow a more detailed investigation to be carried out, of process areas which are major contributors to inherent failure mechanisms, and a more basic study of the physics of failure.

At present it seems that a significant contribution could be made by a study of surface passivation and oxide formation.

If a method of rapid reliability testing was devised giving results which could be extrapolated to the equivalent long term reliability analysis figures then a major contribution to improved reliability could be attained.

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APPENDIX I

The following is a list of publications used in the preparation of this report.

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